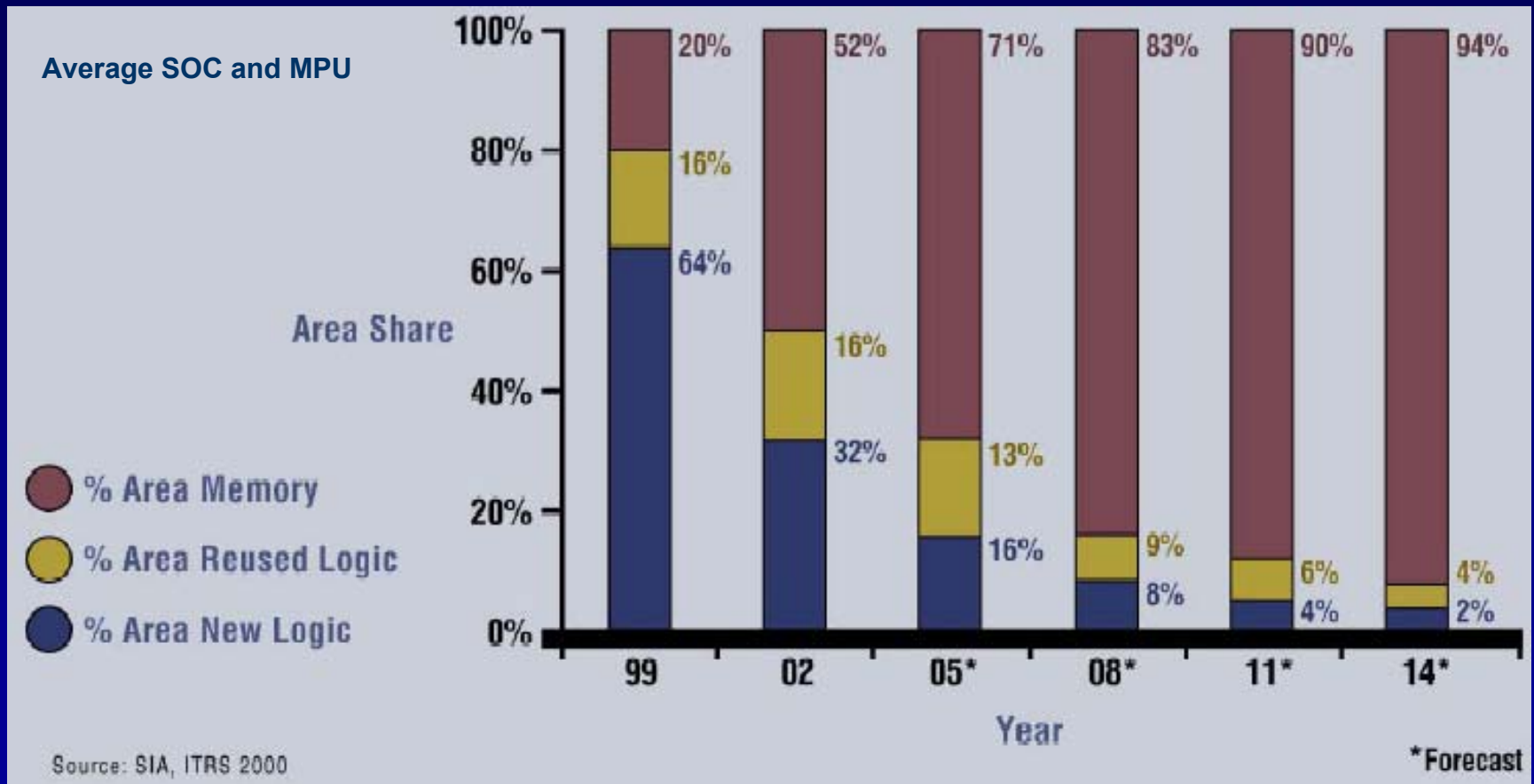


Z-RAM and the Cinderella Effect

Mark-Eric Jones
President & CEO
Innovative Silicon, Inc.

Fall Processor Forum
2005

Embedded memory's changing role



- Embedded memory now dominates die area/cost

**Existing on-chip memory
technologies are reaching
the limits of scaling**

SRAM scaling problems

- Low density: occupies too much die area
- Soft-error rate increasing with process scaling
- Leakage increasing with process scaling

Microprocessor evolution



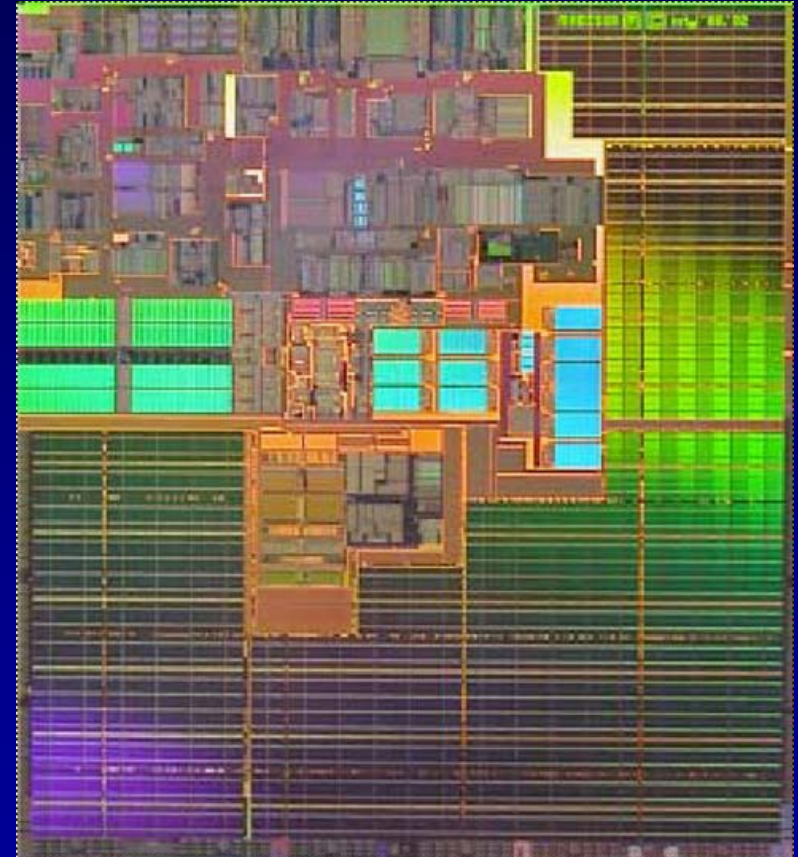
8080

~25mm²

(6μ process)

8080: no caches

**Itanium: caches occupy
68% of die, or ~11x total
8080 die area**

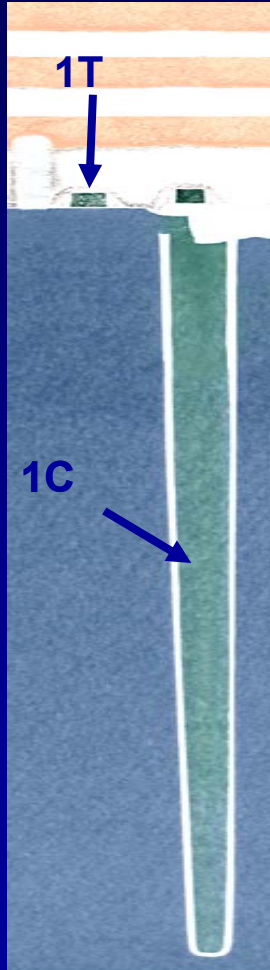


Itanium

~400mm²

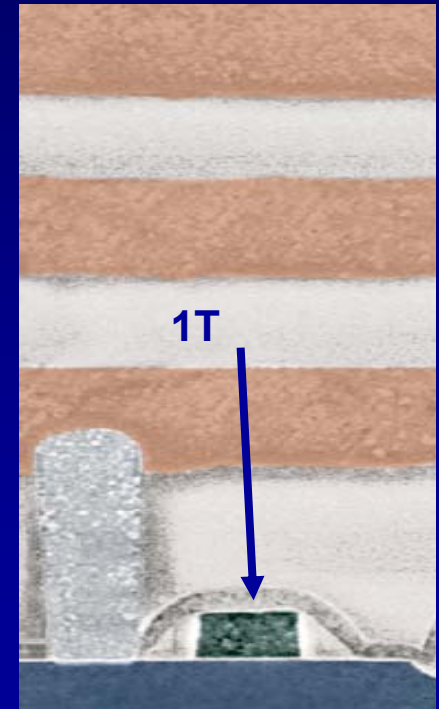
(90nm process)

Scalability challenge for eDRAM

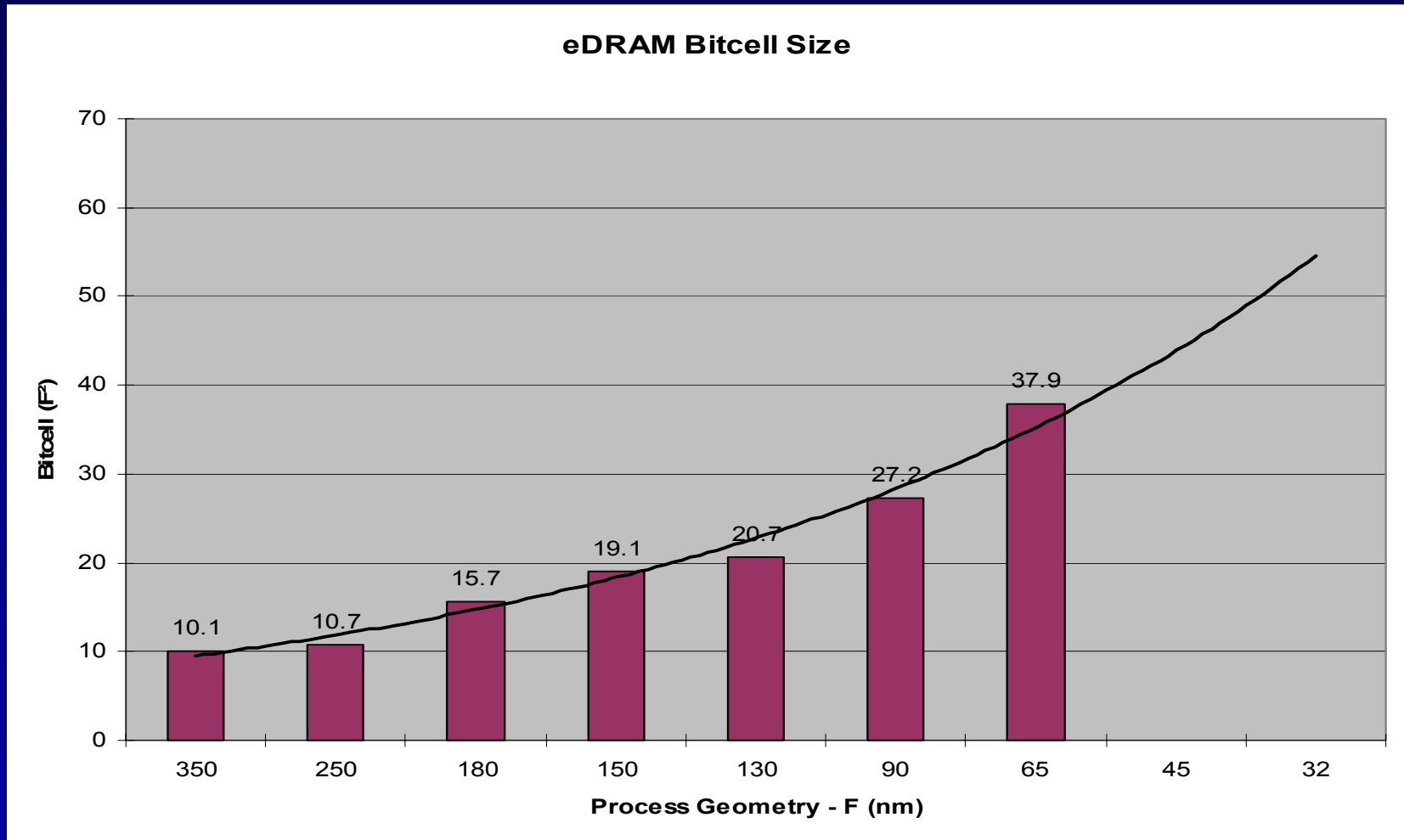


eDRAM

- DRAM trench/stack aspect ratio
 - Huge manufacturing challenge
 - Barrier to scaling beyond 90nm
- Deep trench incompatible with SOI
 - Limits availability on future processes
- High capacitance bit cell
 - Active power penalty

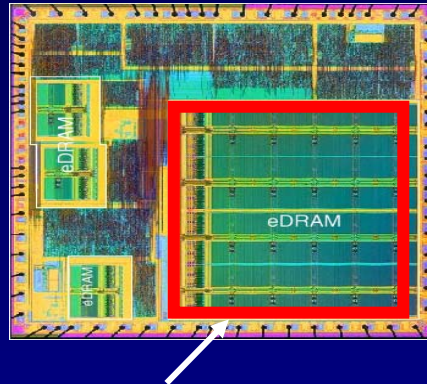


eDRAM reaching the scaling limit

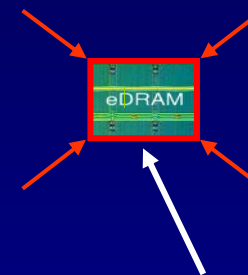


Introducing Z-RAM

ISi's patented memory technology



Traditional embedded memory

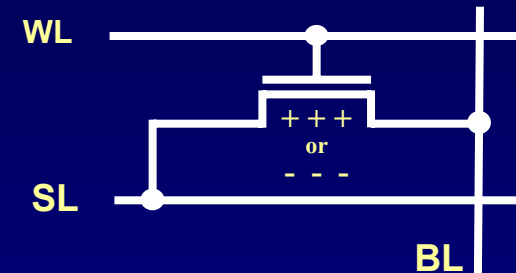


Innovative Silicon's **Z-RAM**
embedded memory technology

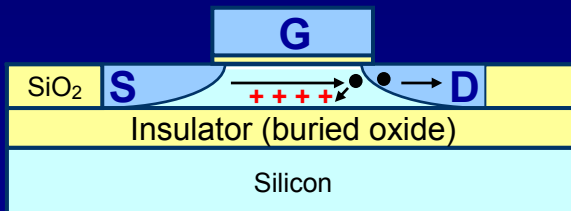
- ISi leverages silicon-on-insulator (SOI) technology to reduce the die area (& hence cost) of memory by **2x** (vs. eDRAM) or **5x** (vs. SRAM) at the same process geometry
- This makes **Z-RAM** the lowest cost of all semiconductor (R/W) memory technologies
- Reverses economics; for most chips this makes SOI lower cost than bulk CMOS
- **Z-RAM** requires no extra steps or masks on standard SOI logic process

Z-RAM bit cell: One transistor, Zero capacitors

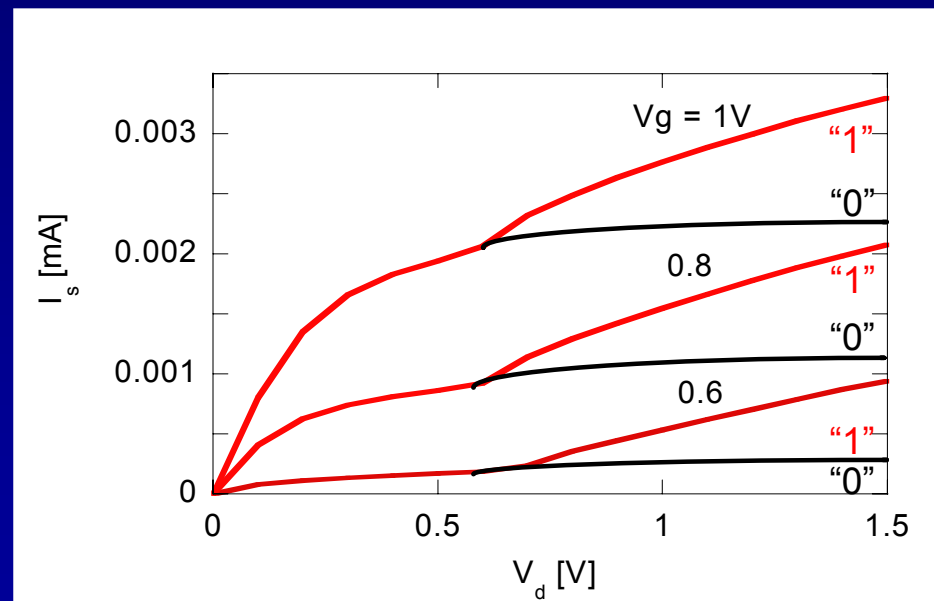
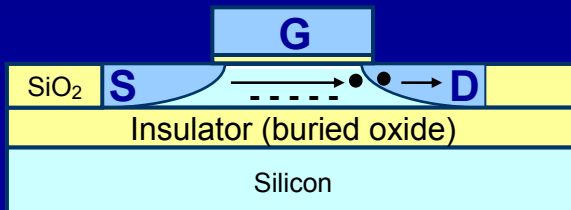
- Exploiting the floating body and gain effects of SOI devices



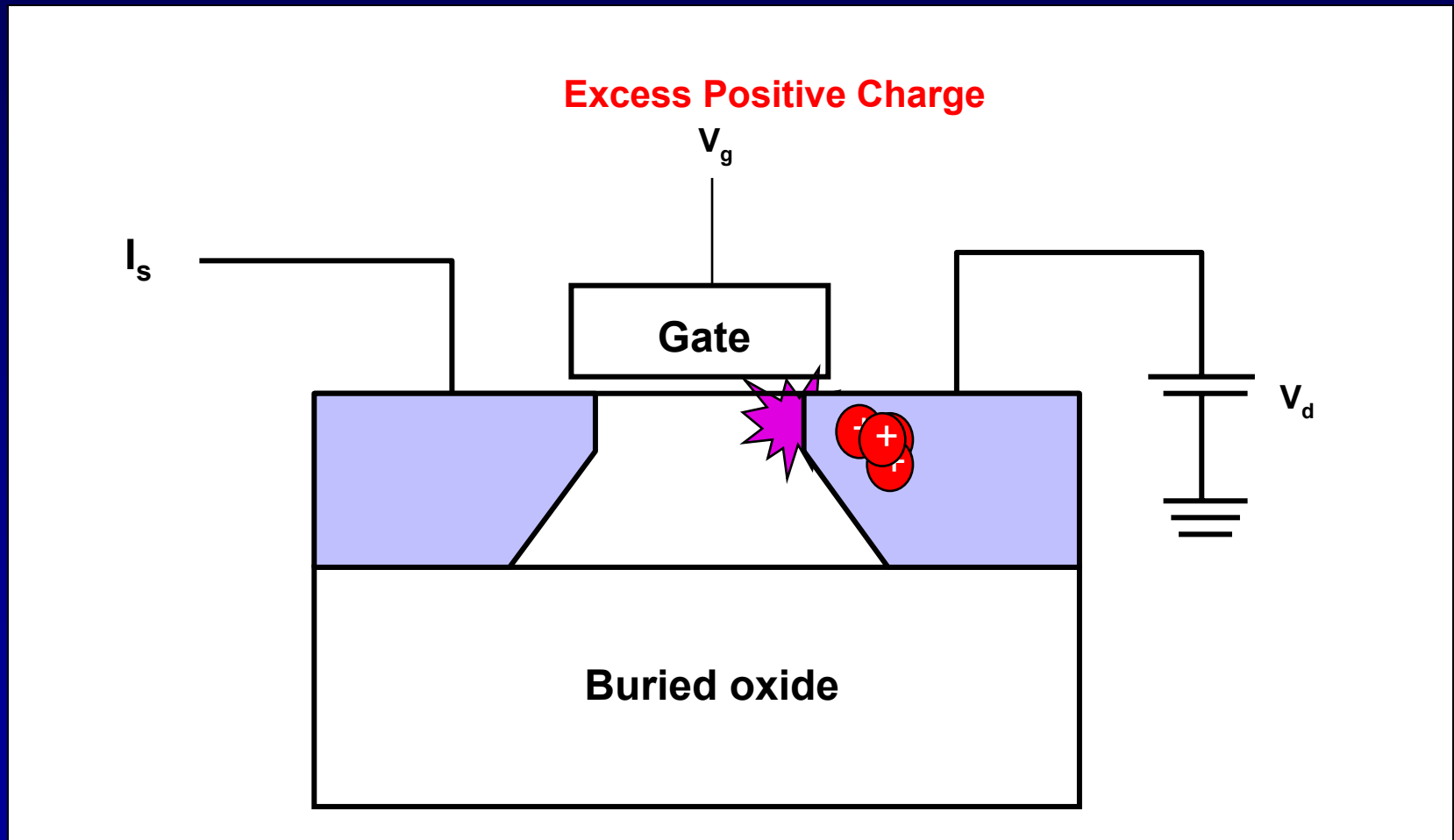
Logic "1"



Logic "0"

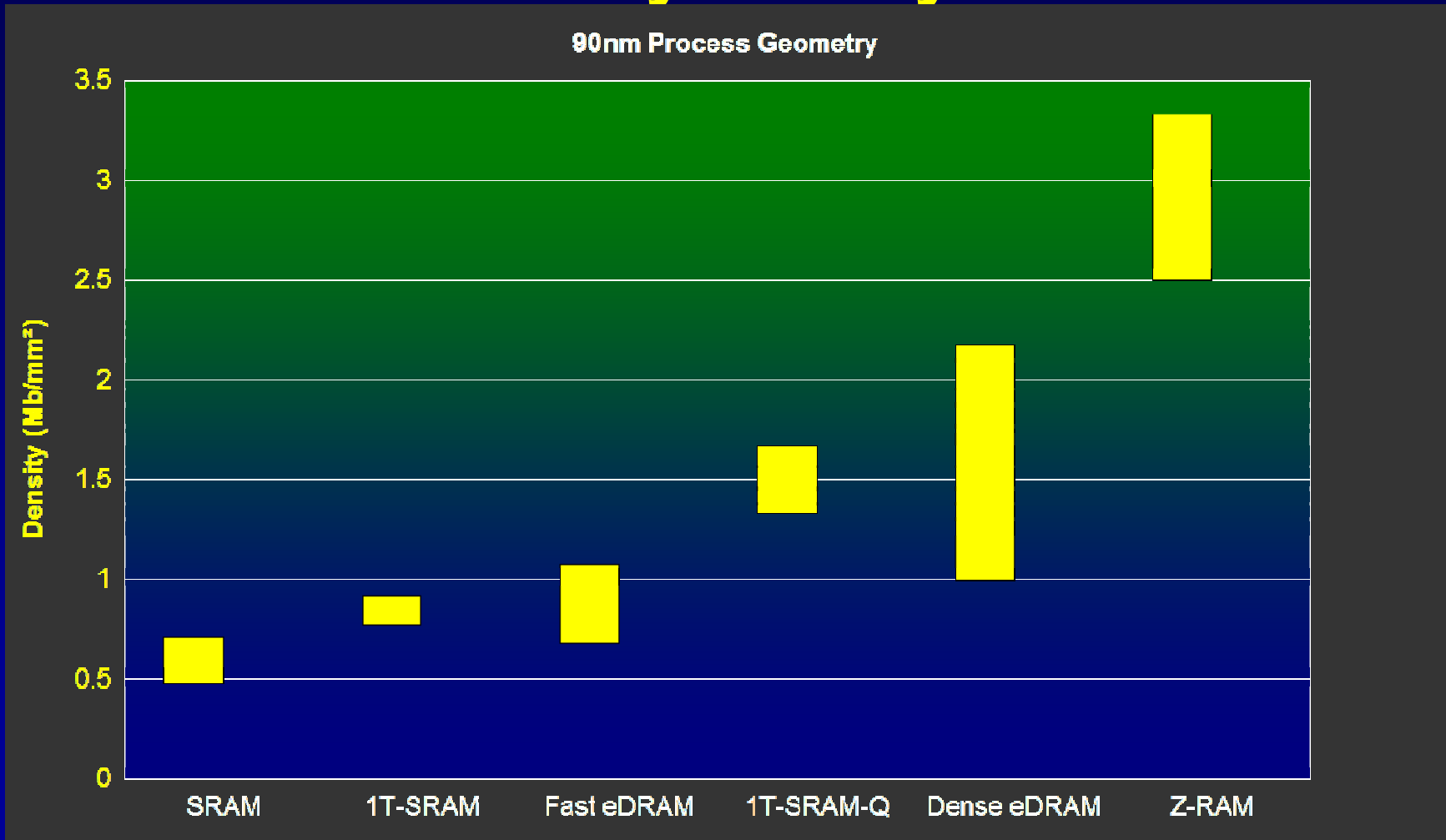


Writing “1” by impact ionization



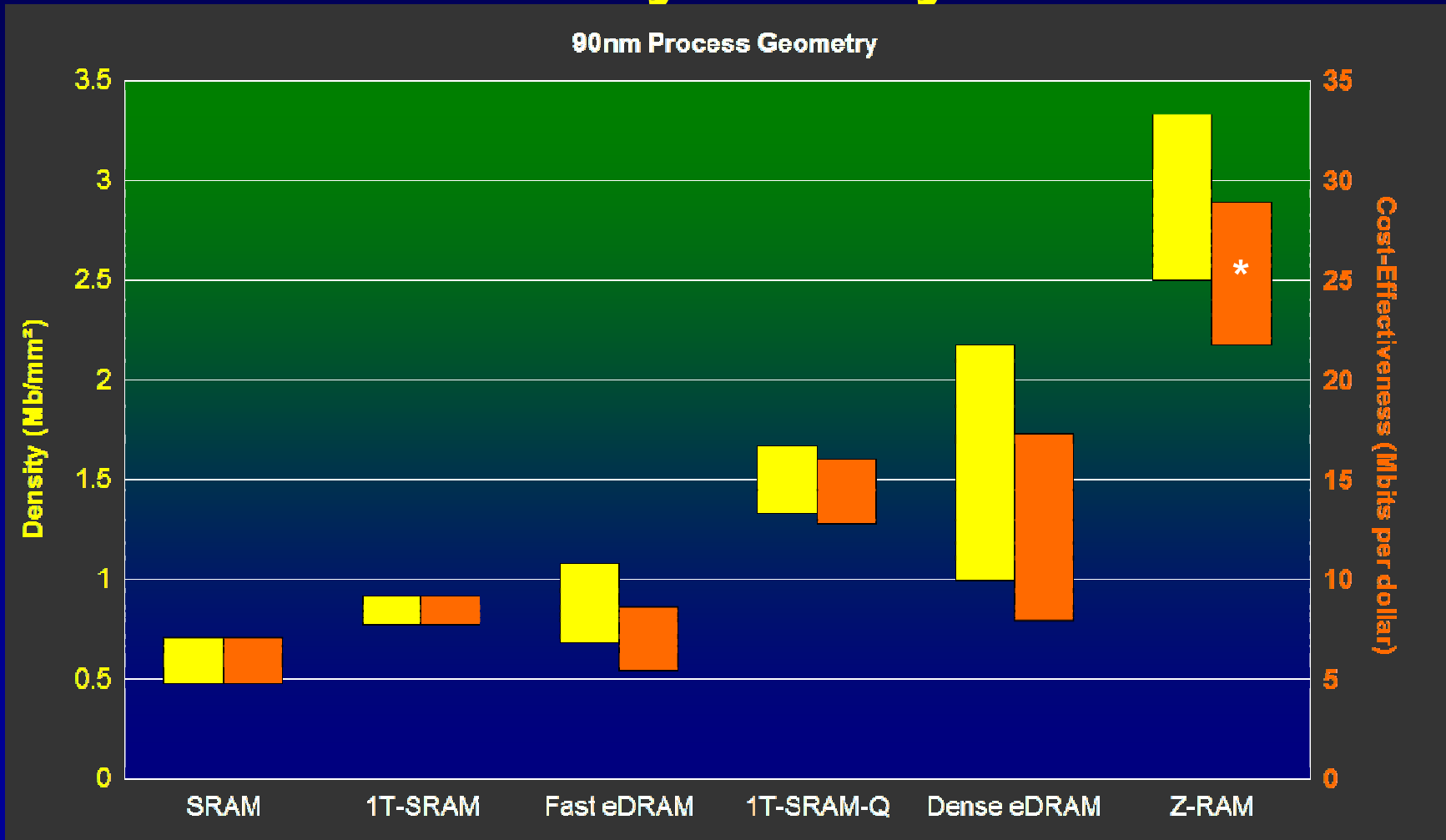


Embedded memory density & economics



1T-SRAM is a registered trademark of MoSys, Inc.

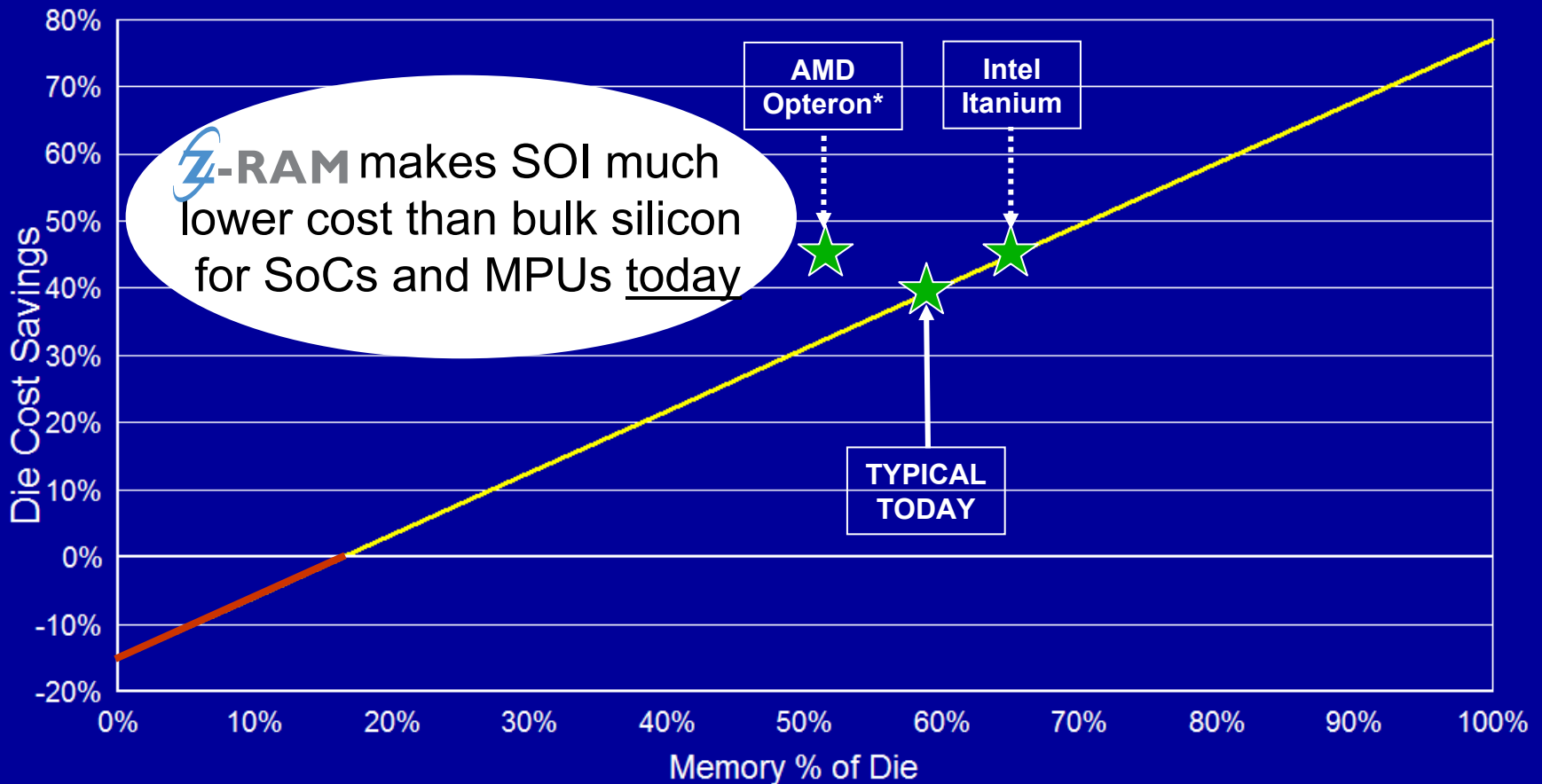
Embedded memory density & economics



* No extra steps, 15% cost increase for SOI vs. bulk silicon wafers

1T-SRAM is a registered trademark of MoSys, Inc.

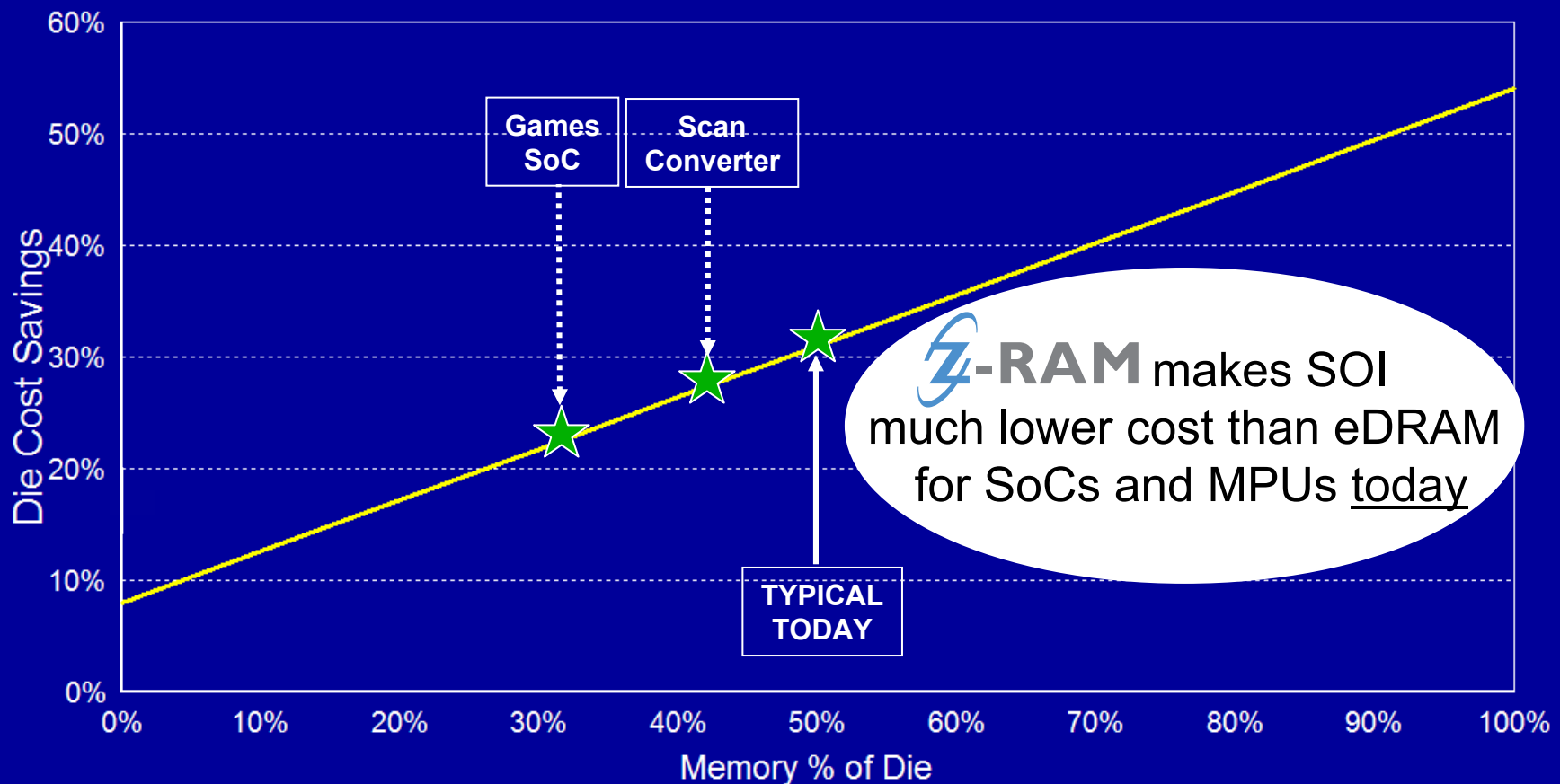
Savings using Z-RAM & SOI vs. SRAM & bulk



Figures assume 15% higher wafer cost for SOI

*AMD Opteron already uses SOI for performance, so savings are 15% higher

Savings using Z-RAM & SOI vs. eDRAM & bulk



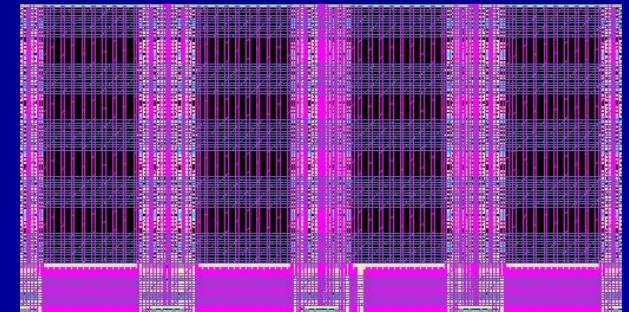
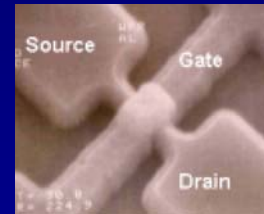
Figures assume 15% higher wafer cost for SOI and 25% higher for eDRAM

Z-RAM high-speed capability


- Demonstrated < 3ns read & write on silicon
- Ultra-high density reduces wire lengths
 - Already faster than eDRAM
 - Promises very high speed as geometries shrink
 - Helps logic speed due to standard SOI logic process and reduced overall chip dimensions

Z-RAM technology status

- Silicon-proven at bit-cell level
 - Demonstrated at nine different foundries
 - Demonstrated down to $L_{\text{phys}} = 40\text{nm}$
 - Demonstrated on Partially Depleted (PD) & Fully Depleted (FD) SOI
 - Demonstrated on FinFET
- Megabit-size test chips fabricated in 90nm process
 - 65nm test chips currently in fab



ISi: IP-licensing business model

- Licensing  **Z-RAM** for embedded use
- Flexible licensing models
 - Instance license
 - Licensee can use memory instance in chip designs
 - Technology license
 - Licensee can develop & modify memory designs themselves
 - Compiler license
 - Licensee can use memory compiler to generate instances

Summary

- Caches are dominating microprocessor die area & cost
- Existing embedded-memory solutions hitting scaling limits
- Ultra-dense, patented **Z-RAM** memory technology
 - Lowest cost, highest density semiconductor memory
 - 2x density of eDRAM, 5x density of SRAM
 - Uses standard SOI logic process
 - No new equipment, no new materials, no extra steps
- Makes SOI lower cost than bulk CMOS today
 - Will accelerate industry transition to SOI
- IP-provider business model
 - Flexible licensing options

Contact

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Ultra-Dense Embedded Memory Technology